In the claims

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13. (Currently amended) [An apparatus] A memory controller, comprising:

a) a host side [memory controller] region having a memory access request input and a memory command packet chunk output, a memory command packet chunk being a portion of a memory command packet, said host side [memory controller] region to be clocked by a first clock; and

B1

b) a memory side [memory controller] region having a memory command packet chunk input coupled to said memory command packet chunk output, said memory side [memory controller] region to be clocked by a second clock, said second clock different than said first clock.

14. (Currently amended) The [apparatus] memory controller of claim 13 wherein said memory command packet chunk output further comprises a row output and a column output.

15. (Currently amended) The [apparatus] memory controller of claim 13 wherein said host side [memory controller] region further comprises a scheduler coupled to said memory access request input, said scheduler configured to generate said memory command packet.

16. (Currently amended) The [apparatus] memory controller of claim 15 wherein said scheduler is coupled to a queue.

17. (Currently amended) The [apparatus] memory controller of claim 15 wherein said memory command packet [is] can be a row command.

18. (Currently amended) The [apparatus] memory controller of claim 15 wherein said memory command packet [is] can be a column command.

19. (Currently amended) The [apparatus] memory controller of claim 15 wherein said scheduler further comprises logic to determine when resource conflicts may arise.

B1

20. (Currently amended) The [apparatus] memory controller of claim 13 wherein said host side memory controller region further comprises a second memory command packet chunk output.

21. (Currently amended) The [apparatus] memory controller of claim 20 wherein said second clock is faster than said first clock.

22. (Currently amended) The [apparatus] memory controller of claim 20 wherein said host side memory controller region is configured to present a second memory command packet chunk upon said second memory command packet chunk output, said second memory command packet chunk a portion of a second memory command packet.

23. (Currently amended) An apparatus, comprising:

a) a memory controller comprising a host side region and a memory side region, said host region having a memory access request input and a memory command packet chunk output, a memory command packet chunk being a portion of a memory command packet, said host side region to be clocked by a first clock, said memory side region having a memory command

packet chunk input coupled to said memory command packet chunk output, said memory side region to be clocked by a second clock, said second clock different than said first clock; and

b) a DRAM memory coupled to said memory side region.

24. (Currently amended) The apparatus of claim 23 further comprising an external agent configured to read and write to said DRAM memory via said memory controller.

25. (Previously presented) The apparatus of claim 24 wherein said external agent further comprises a processor.

26. (Previously presented) The apparatus of claim 24 wherein said external agent further comprises a graphics subsystem.

27. (Previously presented) The apparatus of claim 24 wherein said external agent further comprises an expansion bus master.

28. (Previously presented) The apparatus of claim 23 wherein said memory command packet chunk output further comprises a row output and a column output.

29. (Previously presented) The apparatus of claim 23 wherein said host side memory controller region further comprises a scheduler coupled to said memory access request input, said scheduler configured to generate said memory command packet.

30. (Previously presented) The apparatus of claim 29 wherein said scheduler is coupled to a queue.

31. (Currently amended) The apparatus of claim 29 wherein said memory command packet [is] can be a row command.

32. (Currently amended) The apparatus of claim 29 wherein said memory command packet [is] can be a column command.

33. (Previously presented) The apparatus of claim 29 wherein said scheduler further comprises logic to determine when resource conflicts may arise.

34. (Previously presented) The apparatus of claim 23 wherein said host side memory controller region further comprises a second memory command packet chunk output.

35. (Previously presented) The apparatus of claim 34 wherein said second clock is faster than said first clock.

36. (Previously presented) The apparatus of claim 34 wherein said host side memory controller region is configured to present a second memory command packet chunk upon said second memory command packet chunk output, said second memory command packet chunk a portion of a second memory command packet.

37. (Previously presented) A method, comprising:

a) generated a memory command packet from a memory request while clocked by a first clock; and

b) sending a memory command packet chunk to a memory controller region clocked by a second clock, a memory command packet chunk being a portion of said memory command packet, said second clock different than said first clock.

38. (Previously presented) The method of claim 37 further comprising sending a second memory command packet chunk along with said memory command packet chunk, said second memory command packet chunk associated with a subsequent memory command packet.

39. (Previously presented) The apparatus of claim 37 wherein said memory command packet further comprises a row command.

B1

40. (Previously presented) The apparatus of claim 39 wherein said row command activates a memory row.

41. (Previously presented) The apparatus of claim 39 wherein said row command precharges a memory row.

42. (Previously presented) The apparatus of claim 39 wherein said memory command packet further comprises a column command.

43. (Currently amended) The apparatus of claim 39 wherein said column command is use to read from a DRAM memory device.

44. (Currently amended) The apparatus of claim 39 wherein said column command is used to write to a DRAM memory device.

45. (new) A memory controller, comprising:

a) a host side region to be clocked by a first clock, said host side region comprising:

(i) a queue to queue command packet chunks;

(ii) a plurality of memory command packet chunk output lanes stemming from steering circuitry, said steering circuitry to guide specific command packet chunks received from

said queue to specific command packet chunk output lanes, said queue having an output for each output lane, said steering circuitry further comprising:

a) a first multiplexer having a first input to receive a first packet chunk from a queue output, said first multiplexer having a second input coupled to a latch circuitry output, said latch circuitry downstream from said queue output to hold a second packet chunk from said queue output;

b) a second multiplexer having a plurality of inputs, one of said inputs coupled to said first multiplexer's output, other inputs of said second multiplexer downstream from outputs of said queue other than said queue output; and,

b) a memory side region to be clocked by a second clock, said memory side region comprising:

inputs coupled to said memory command packet chunk output lanes.

46. (new) The memory controller of claim 45 further comprising shift logic on said memory side region to receive memory command packet chunks from said memory side region inputs.

47. (new) The memory controller of claim 45 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

48. (new) The memory controller of claim 45 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

49. (new) The memory controller of claim 45 further comprising a third multiplexer having a first input coupled to said queue output and a second input coupled to a path that propagates command packets chunks that do not enter said queue, said latch circuitry coupled to said third multiplexer's output to receive command packet chunks from said third multiplexer's output.

50. (new) The memory controller of claim 49 wherein said third multiplexer further comprises a third input coupled to an output of said latch circuitry.

51. (new) The memory controller of claim 45 wherein said steering circuitry further comprises a third multiplexer having a first input coupled an output of said second multiplexer, said third multiplexer having a second input coupled to a path that propagates command packets chunks that do not enter said queue.

52. (new) The memory controller of claim 51 further comprising logic circuitry between said third multiplexer and an output lane to insert a null packet chunk onto said output lane.

53. (new) An apparatus, comprising:

a memory controller, comprising:

a) a host side region to be clocked by a first clock, said host side region comprising:

(i) a queue to queue command packet chunks;

(ii) a plurality of memory command packet chunk output lanes stemming from steering circuitry, said steering circuitry to guide specific command packet chunks received from said queue to specific command packet chunk output lanes, said queue having an output for each output lane, said steering circutry further comprising:

a) a first multiplexer having a first input to receive a first packet chunk from a queue output, said first multiplexer having a second input coupled to a latch circuitry output, said latch circuitry downstream from said queue output to hold a second packet chunk from said queue output;

b) a second multiplexer having a plurality of inputs, one of said inputs coupled to said first multiplexer's output, other inputs of said second multiplexer downstream from outputs of said queue other than said queue output;

B1

b) a memory side region to be clocked by a second clock, said memory side region comprising:

inputs coupled to said memory command packet chunk output lanes; and,

DRAM memory coupled to said memory side region of said memory controller.

54. (new) The apparatus of claim 53 further comprising shift logic on said memory side region to receive memory command packet chunks from said memory side region inputs.

55. (new) The apparatus of claim 53 wherein said steering circuitry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

56. (new) The apparatus of claim 53 wherein said steering circutry is to guide specific row command packet chunks to said specific command packet chunk output lanes, said queue to queue row command packet chunks.

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57. (new) The apparatus of claim 53 further comprising a third multiplexer having a first input coupled to said queue output and a second input coupled to a path that propagates command packets chunks that do not enter said queue, said latch circuitry coupled to said third multiplexer's output to receive command packet chunks from said third multiplexer's output.

58. (new) The apparatus of claim 57 wherein said third multiplexer further comprises a third input coupled to an output of said latch circuitry.

59. (new) The apparatus of claim 53 wherein said steering circuitry further comprises a third multiplexer having a first input coupled an output of said second multiplexer, said third multiplexer having a second input coupled to a path that propagates command packets chunks that do not enter said queue.

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60. (new) The apparatus of claim 59 further comprising logic circuitry between said third multiplexer and an output lane to insert a null packet chunk onto said output lane.

COMMENTS

The enclosed is responsive to the Examiner's Office Action mailed on June 3, 2003. At the time the Examiner mailed the Office Action claims 13 - 44 were pending. By way of the present response the Applicant has: 1) amended claims 13-24, 31, 32, 43 and 44; and, 2) added new claims 45 through 60. As such claims 13 - 60 remain pending. The Applicant respectfully requests reconsideration of the present application and the allowance of claims 13 - 60.

The Examiner has maintained a theory of rejection that the disclosure of US Patent No. 6,000,022 (hereinafter, "Martin") is sufficient to anticipate each and every one of the Applicant's claims under 35 USC 102(e). As part of the theory of rejection the Examiner has effectively reasoned that: 1) the teachings of Col. 5, line 65 to Col. 6, line 12 of Martin are sufficient to cover the Applicant's claim element "a memory command packet chunk output" (See, Office Action mailed 6/3/03, pg. 2); and, 2) the teachings of Col. 1, line 51 to Col. 2, line 5 of Martin are sufficient to cover "a memory command packet chunk input coupled to [the] memory command packet chunk output".

Notably, the pair of Office Actions sent by the Examiner prior to the outstanding Office Action (i.e., a First Office Action mailed 12/03/02 and a Final Office Action mailed 3/18/03) stated nothing more than "Figure 2" of Martin anticipated the Applicant's claims (See, Office Action mailed 12/03/02, pg. 2 and Final Office Action mailed 3/18/03, pgs. 2-3). Yet, in response to the Examiner having been pushed by the Applicant to provide a more thorough articulation of the Examiner's precise reasoning (See, Applicant's response to Final Office Action mailed 5/12/03, pg. 2), which was nothing more than a request for the Examiner to articulate what was supposed to have been articulated at the onset (See, MPEP 2131), the Examiner presently responds to the Applicant with justifications for rejection that do not in any way refer to Figure 2 of Martin. Specifically, Col. 5, line 65 to Col. 6, line 12 of Martin clearly refers to Figure 3 of Martin; and, Col. 1, line 51 to Col. 2, line 5 of Martin does not refer to any of the figures of Martin (acting mostly as a preface to the discussion surrounding Figure 1 of Martin).

With the Examiner's true theory of rejection having been revealed so as to depend from subject matter outside the realm of Figure 2 of Martin, making plain that the Examiner's previous efforts regarding the prosecution of the present application has done nothing more than waste eight months of the lifetime of the Applicant's patent (above and beyond the two years and nine months consumed waiting for a first office action) and waste $750 of the Applicant's money for a Request for Continued Examination (RCE) by refusing allowance only with "Figure 2" of Martin as a sole basis for rejection, the Applicant respectfully submits that, at a minimum, the Examiner owes the Applicant another non-Final response irrespective of the claim amendments that have been presently filed herewith.

Moreover, the Examiner's theory of rejection as stated in the currently outstanding Office Action is insufficient to refuse allowance of the Applicant's claims for at least those reasons described in detail immediately below.

First and foremost, each of the Applicants claims include elements directed to a "memory controller" whereas Martin is limited to describing a "memory". As succinctly stated in the following excerpts from the Applicant's specification (as it refers to Figure 1 of the Applicant's specification):

> "Fig. 1 illustrates a memory system 10 according to one embodiment. The memory system 10 includes a memory controller 20 [and] a memory array 11... "
>
> "The memory controller 20 includes host-side control logic 21, memory-side control logic 22 and gear logic 23."
>
> "The host side control logic 21 includes a scheduler 30 that receives requests to read and write the memory array 11 from external agents (e.g., processor, graphics subsystem, expansion bus master, and so forth). In one embodiment, the memory array 11 is a dynamic random access memory (DRAM) . . . "
>
> Applicant's Specification pg. 6, lines 24-25; pg. 7, lines 7-9 and 18-22, respectively.

Therefore, as the Applicant's claims explicitly say, the Applicant's claims are directed to a memory controller.

By contrast, Martin only describes in detail the inner workings of a memory. Therefore it is impossible for Martin to **anticipate** the Applicant's claims. See, MPEP 2131. That the detailed description of the various circuitry of Martin is limited to a memory rather than a memory controller is made clear through at least the following observations:

> 1) Martin discloses that DRAM memory devices are "too slow" as compared to the speed of processor devices; and, that a memory controller helps to allow a faster processor to communicate with a slower DRAM memory (See, Col. 1, line 19 through Col. 2, line 5 of Martin; and, in particular, Col. 1, lines 26 – 34 and Col. 1, line 64 through Col. 2, line 1 of Martin);
>
> 2) Martin discloses that an approach that aims to alleviate the speed problem described above is a "SyncLink" architecture that employs the use of command packet and that does not include a memory controller (See, Col. 2, lines 6 – 39 of Martin; and, in particular Col. 2 lines 8 – 10 of Martin and Figure 1 of Martin).
>
> 3) Martin makes clear that the invention of Martin is directed to a design for a memory that is to process command packets consistent with the SyncLink architectural approach (See, Col. 4, lines 22 – 64 and Col. 5, lines 55 – 64 of Martin; and, in particular, Col. 4, lines 22-24 and 43 – 58 of Martin.
>
> 4) Figure 2 of Martin is explicitly referred to as a memory device and not as a memory controller;
>
> 5) Martin never again refers to the term memory controller once the initial discussion regarding the speed disparity between processors and memory devices (which ends at Col. 2, line 5) that precedes the discussion of Figure 1 is complete.

Consistent with the realizations provided above, the Examiner has attempted to invalidate claim elements directed to a host side of a memory controller ("a host side memory controller region having a memory command packet chunk output") with material from Martin directed to the input circuitry of a memory. Specifically, Col. 5, line 65 to Col. 6, line 12 of Martin (which the Examiner has used to cover the

claim element at issue) refers to the "memory device 200 presented in Figure 3" of Martin (See, Martin, Col. 55, lines 55-56); and, therefore, not to a memory controller. Therefore, it is impossible for Martin to anticipate this particular claim element. The claim amendments being presented herewith do not change this situation.

Moreover, the Examiner has attempted to invalidate claim elements directed to a memory side of a memory controller that can receive command packets in chunks ("a memory side memory controller region having a memory command packet chunk input") with material from Martin that fails to disclose a chunk of a packet or the memory side of a memory controller. Specifically, the teachings of Col. 1, line 51 to Col. 2, line 5 of Martin (which the Examiner has used to cover the claim element at issue), as discussed above, only teaches that DRAM memory devices are "too slow" as compared to the speed of processor devices; and, that a memory controller helps to allow a faster processor to communicate with a slower DRAM memory.

The Applicant respectfully submits that the Examiner's attempt to cover host side memory controller output circuitry with memory device input circuitry and to cover a memory side of a memory controller that can receive command packets in chunks with information that does not disclose command packet chunks or a memory side of a memory controller, is a per se insufficient legal theory to anticipate the Applicant's independent claims 13, 23, and 37. Therefore each of the Applicant's independent claims are allowable and, likewise, all pending claims are allowable.